

Alak Majumder

Assistant Professor, Department of ECE

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Room No - 213, Integrated Circuit & System Lab

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EDUCATION:

NIT Arunachal Pradesh, India — *PhD*

SEPTEMBER 2014 - SEPTEMBER 2018

Area: High Speed Data Link (Major - VLSI)

NIT Agartala, India — *M-Tech*

JULY 2011 - MAY 2013

Specialization: Microelectronics & VLSI Design.

TIT Agartala (Under Tripura University), India — *B-Tech*

JULY 2007 - MAY 2011

Course: Electronics & Telecommunication Engineering.

SPONSORED PROJECTS:

SMDP C2SD — Air Quality Monitoring System (Cluster with IITG)
Digital Smart Card System (Individual)

Agency: Ministry of Electronics & Information Technology, Govt. of India.

Funding: ~ 3.7 Million INR + EDA Lab Setup

RESEARCH INTERESTS & HIGHLIGHTS:

Interests: Analog/Digital IC, Low Power Techniques, Current Mode Design, Wireline Communication Circuit, Clock Distribution & Gating Logic, System Design

Highlights:

No. of Sponsored Projects — 01 (*Ongoing*)

No. of Patents — 05 (*Filed*) & 03 (*Pending*)

No. of Journals — 28 (*Published*) & 10 (*Submitted*)

No. of Conferences — 40

No. of Book Chapters — 02

No. of Books — 00

No. of Project Fellows — 03 (*Ongoing*)

No. of M-Tech Thesis— 16 (*Awarded*), 00 (*Ongoing*)

No. of B-Tech Thesis — 10 (*Awarded*), 02 (*Ongoing*)

Cited By:

	<i>All</i>	<i>Since 2013</i>
<i>Citations</i>	209	208
<i>H - Index</i>	8	8
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AWARDS & HONORS:

Best Research Award, IETE Ash-Tech 2018, Indore, India
Medal and Plaque (30th October 2018)

Best Paper Award, 16th ICEIC 2017, Phuket, Thailand
GOLD Medal and Honorarium of 100USD (11th – 14th January 2017)

Best Hardware Project, Advanced Traffic Monitoring
Gold Medal for B-Tech Project under my Supervision (May 2016)

GATE Qualified, in Electronics & Comm. at 2011 & 2013

SKILLS:

Programming Languages:

VERILOG, VHDL

Logic Simulator (Frontend):

XILINX VIVADO

Circuit Simulator (Backend):

VIRTUOSO WITH SPECTRE (Cadence)
CUSTOM COMPILOR HSPICE (Synopsys)
PYXIS WITH ELDO (Mentor Graphics)

Layout Analyzer (Backend):

DRC/LVS USING ASSURA & RCX USING QUANTUS (Cadence)
DRC/LVS/RCX USING IC VALIDATOR & HERCULES (Synopsys)
DRC/LVS/RCX USING CALIBRE (Mentor Graphics)

PROFESSIONAL SERVICES:

Reviewer of Journals:

INTEGRATION, THE VLSI JOURNAL, ELSEVIER
IEEE TRANSACTIONS ON CAD (TCAD)
IEEE TRANSACTIONS ON NANOTECHNOLOGY
IEEE CONSUMER ELECTRONICS MAGAZINE
MICROELECTRONICS JOURNAL, ELSEVIER
JCSC, WORLD SCIENTIFIC
INT. J. ELECTRONICS, TAYLOR & FRANCIS
INDIAN JOURNAL OF PURE & APPLIED PHYSICS
JOURNAL OF LOW POWER ELECTRONICS, ASP
JMSTE, EURASIA
SEMICONDUCTOR SCIENCE & TECHNOLOGY, IOP
APPLIED COMPUTING & INFORMATICS, ELSEVIER

Organizer/Reviewer of Conferences:

IFSA MicDAT – 2018, BARCELONA, SPAIN
IEEE ICECCOT-2018, MYSURU, INDIA
IEEE INDICON – 2018, IIT ROORKEE, INDIA
IEEE ICCE – 2018, LAS VEGAS, USA
IEEE iNIS/iSES-2016/17/18, HYDERABAD, INDIA
IEEE CICT-2017, GWALIOR, INDIA
IEEE IESC – 2017, SHILLONG, INDIA
IEEE ICECCOT-2017, MYSURU, INDIA
IEEE ICECS – 2016, MONACO, FRANCE
IEEE MWSCAS-2016, ABU DHABI, UAE
IEEE RAECs-2015, CHANDIGARH-INDIA
SPRINGER IC3T-2015, HYDERABAD
IEEE ICIC-2015, PUNE, INDIA
IEEE ICACCE-2015, DEHRADUN, INDIA

MEMBERSHIPS:

MEMBER IEEE, USA
MEMBER IACSIT, SINGAPORE
MEMBER IAENG, HONGKONG
ASSOCIATE MEMBER UACEE

WORKSHOP ORGANIZED:

TAPE OUT FLOW OF ASIC (25th – 30th Jun'18)
VLSID - 18 (12th – 16th Jan' 18)
XILINX VIVADO (30th Sept – 1st Oct' 17)
RECENT TRENDS VLSI (16th–22nd Sept'15)
VLSI DESIGN (Nov' 2013)

ADMINISTRATIVE DUTY:

ASSOCIATE WEBMASTER (Feb'18 – Till Date)
WARDEN, Rose Hall (Dec'17 – Till Date)